



MS-7297 Ver:0D

CPU:

AMD K8 AM2 Athlon 64/Athlon 64 FX

System Chipset:

ATI RS485

ATI SB600

On Board Chipset:

Winbond Super I/O -- W83627EHG Ver.H

LAN -- RTL8100C/RTL8110SC

HD Codec --ALC861

BIOS --LPC FLASH ROM 4M

Main Memory:

DDR2 * 2 (Max 4GB)

Expansion Slots:

PCI-E X 1 *1

PCI-E X 16 *1

PCI 2.3 Slot X 2

PWM:

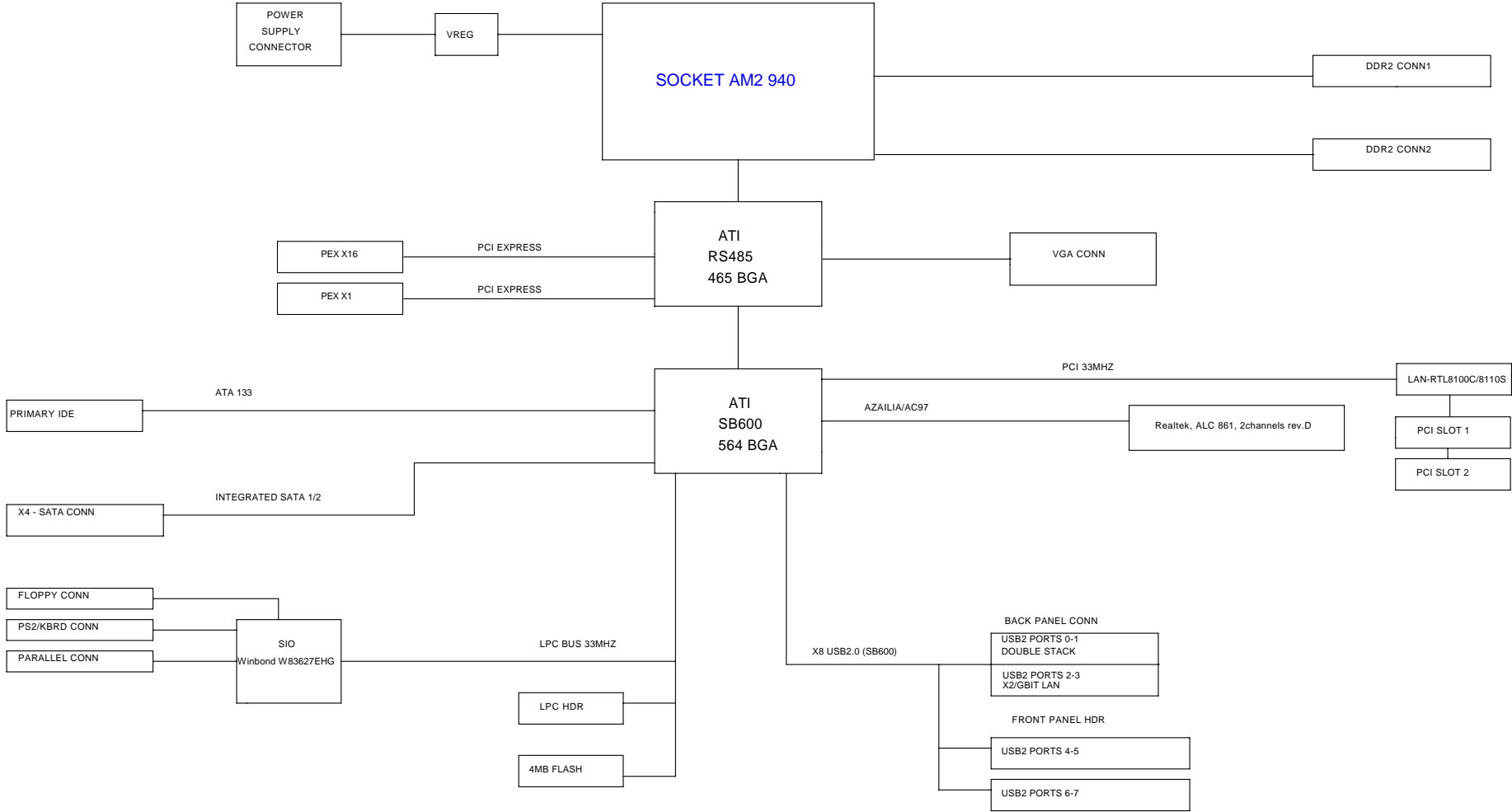
Controller--Intersil ISL6566CR 3 Phase

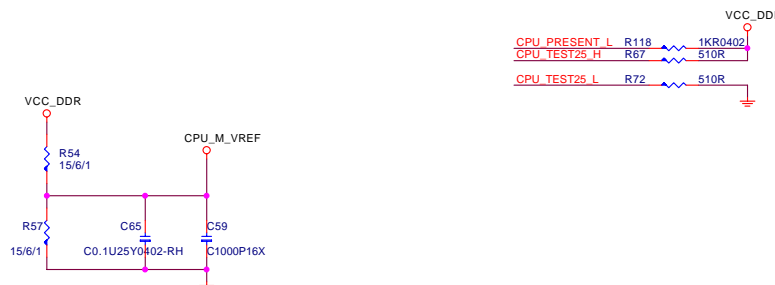
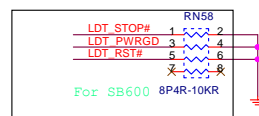
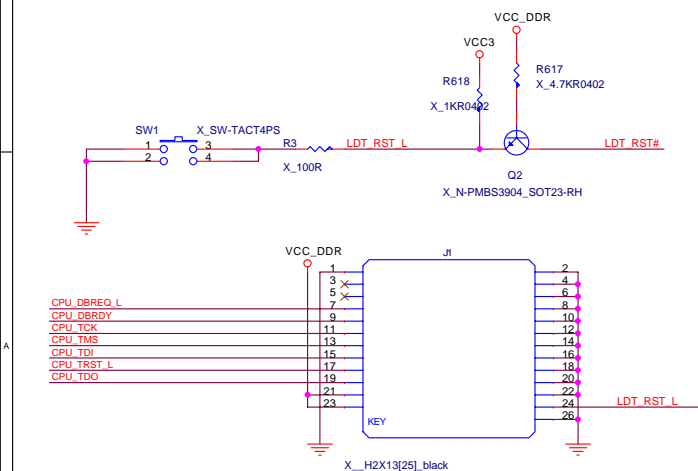
Clock Generator:

Controller--ICS 951464AGLF

Title	Page
Cover Sheet	1
Block Diagram	2
AMD K8 AM2 940	3,4,5
System Memory	6
DDR Terminations	7
ATI RS485	8-11
CLOCK GENERATOR ICS951464AGLF	12
ATI SB600	13-17
PCI Slot 1,2	18
PCI-Express X 16 ,X1	19
I/O W83627EHG Ver.H / FDD	20
LAN RTL8100C/RTL8110SC	21
HD Audio - ALC861	22
USB connectors	23
PWM - ISL6566CRZ 3 phase,TPD=89W	24
MS-6 ACPI Controller & MS-6+	25-26
IDE / SATA / FAN / LPT	27
ATX Connector / Front Panel / KB / CON	28
MANUAL PARTS	29
TV-OUT & VGA Connector	30
GPIO SPEC	31
POWER MAP	32
POWER OK MAP	33
History	34
RESET MAP	35

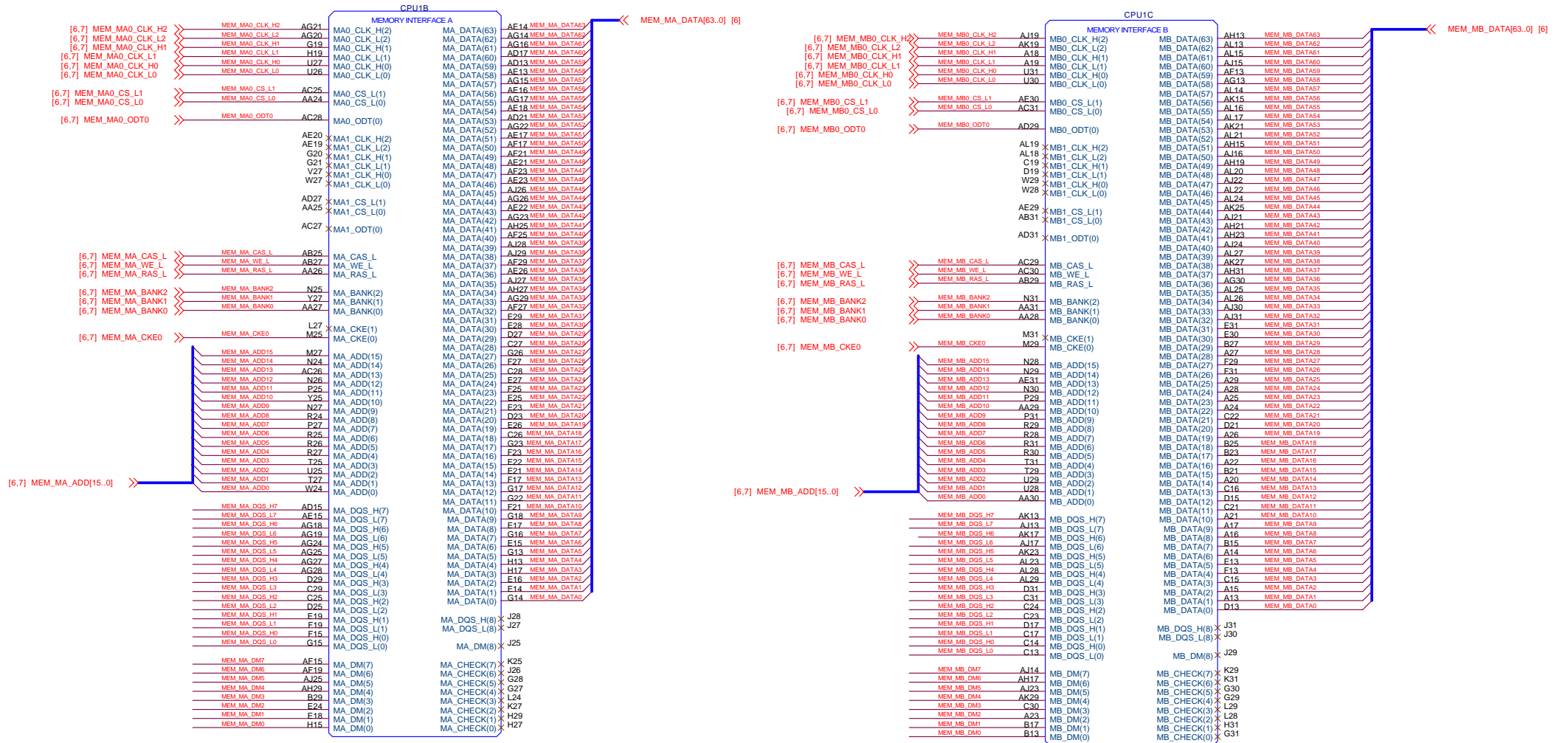
BLOCK DIAGRAM

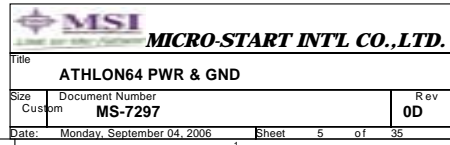




[6] MEM_MA_DQS_L[7..0] >> _____
[6] MEM_MA_DQS_H[7..0] >> _____
[6] MEM_MA_DM[7..0] >> _____

[6] MEM_MB_DQS_L[7..0] >> _____
[6] MEM_MB_DQS_H[7..0] >> _____
[6] MEM_MB_DM[7..0] >> _____



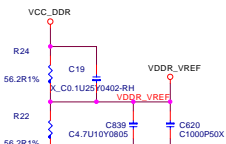


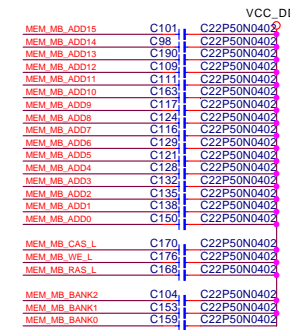
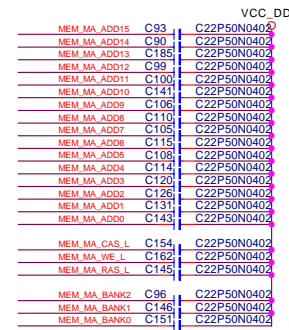
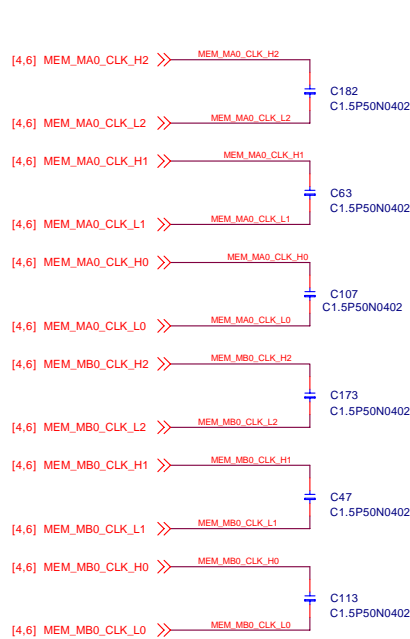
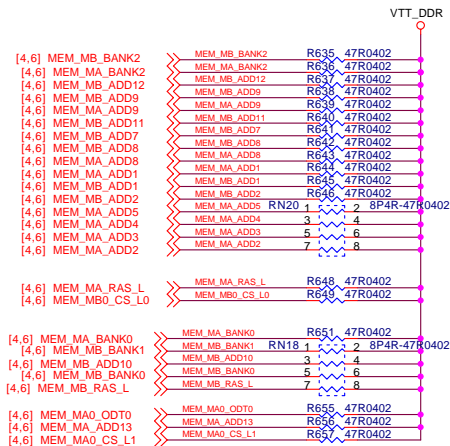
```
DIMM 1
ADDR=1010000B
```

```
DIMM 2
ADDR=1010001B
```

[12,14,20,21,25] SCL<<< SCL R145 33R SCL CLK

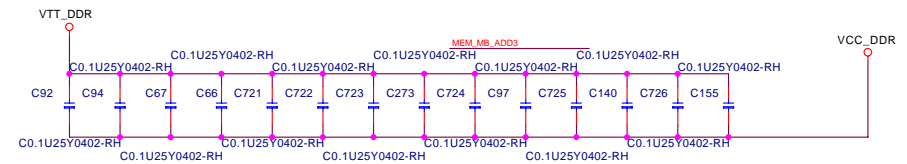
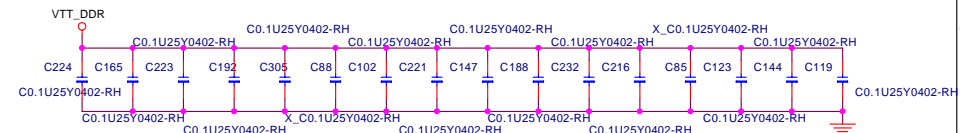
[12,14,20,21,25] SDA<<< SDA R154 33R SDA DATA



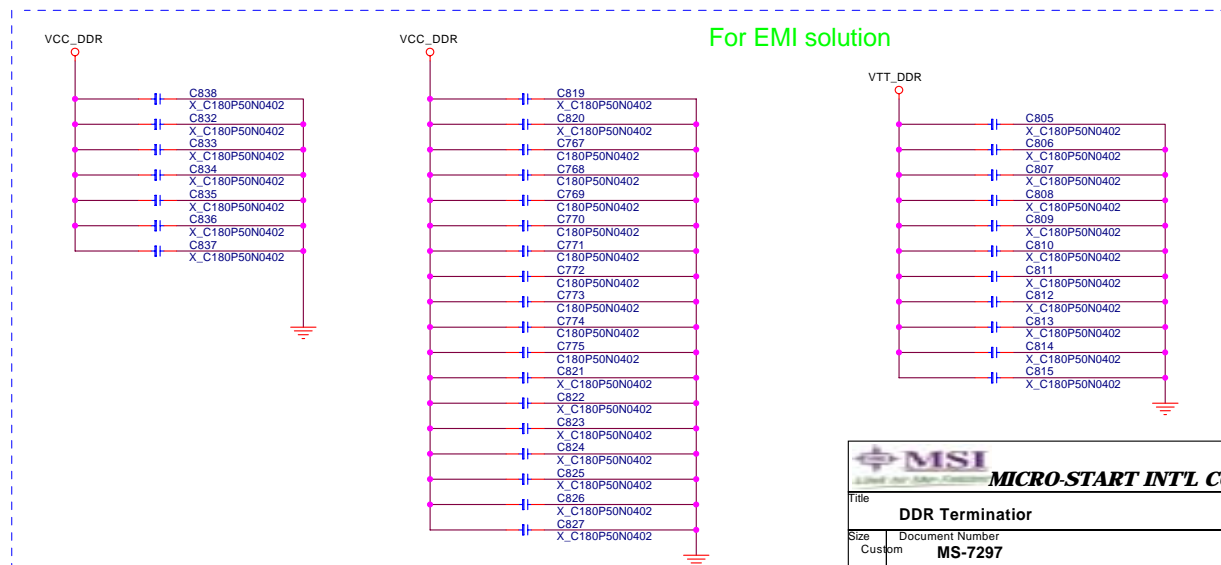


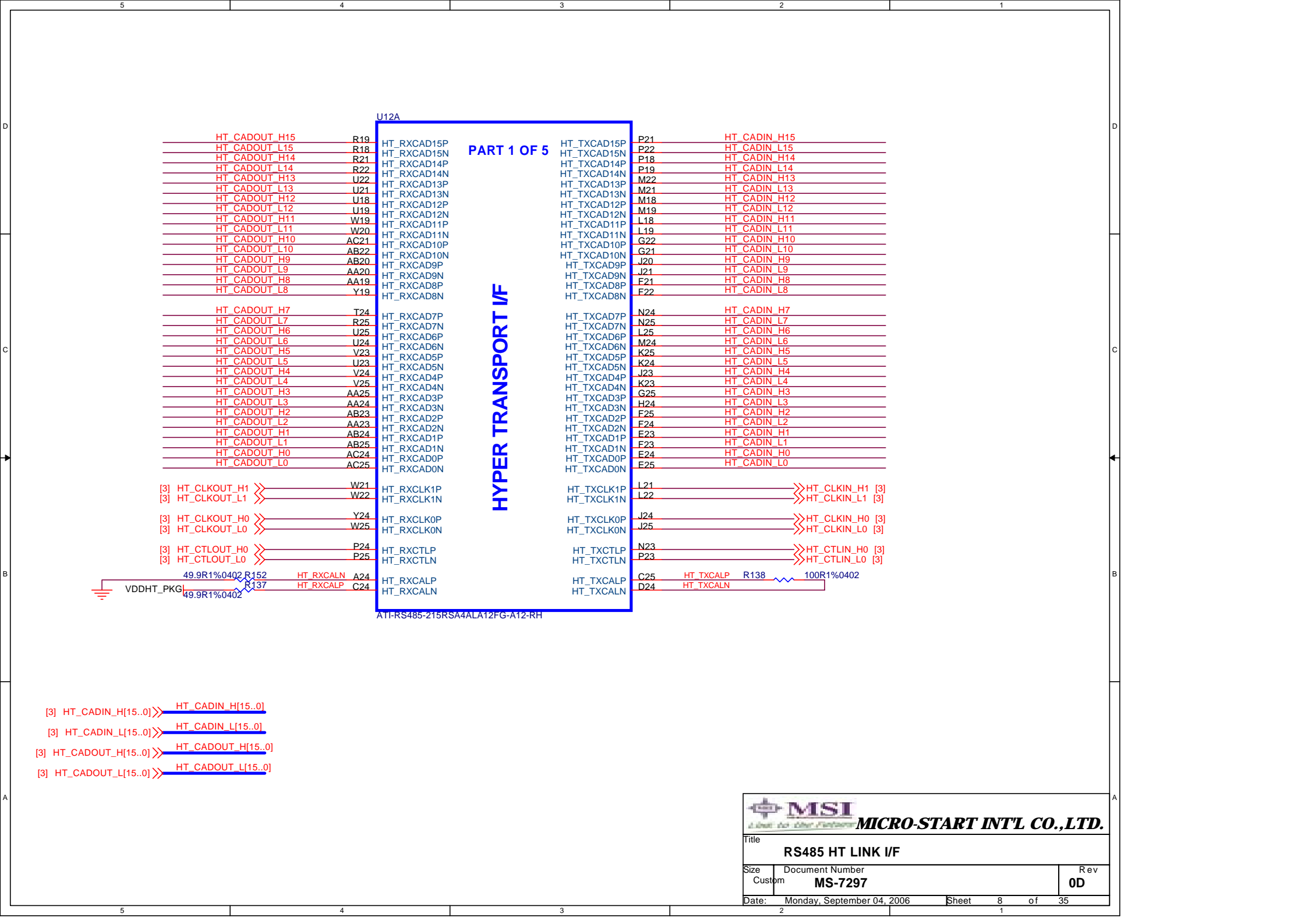
Decoupling Between Processor and DIMMs

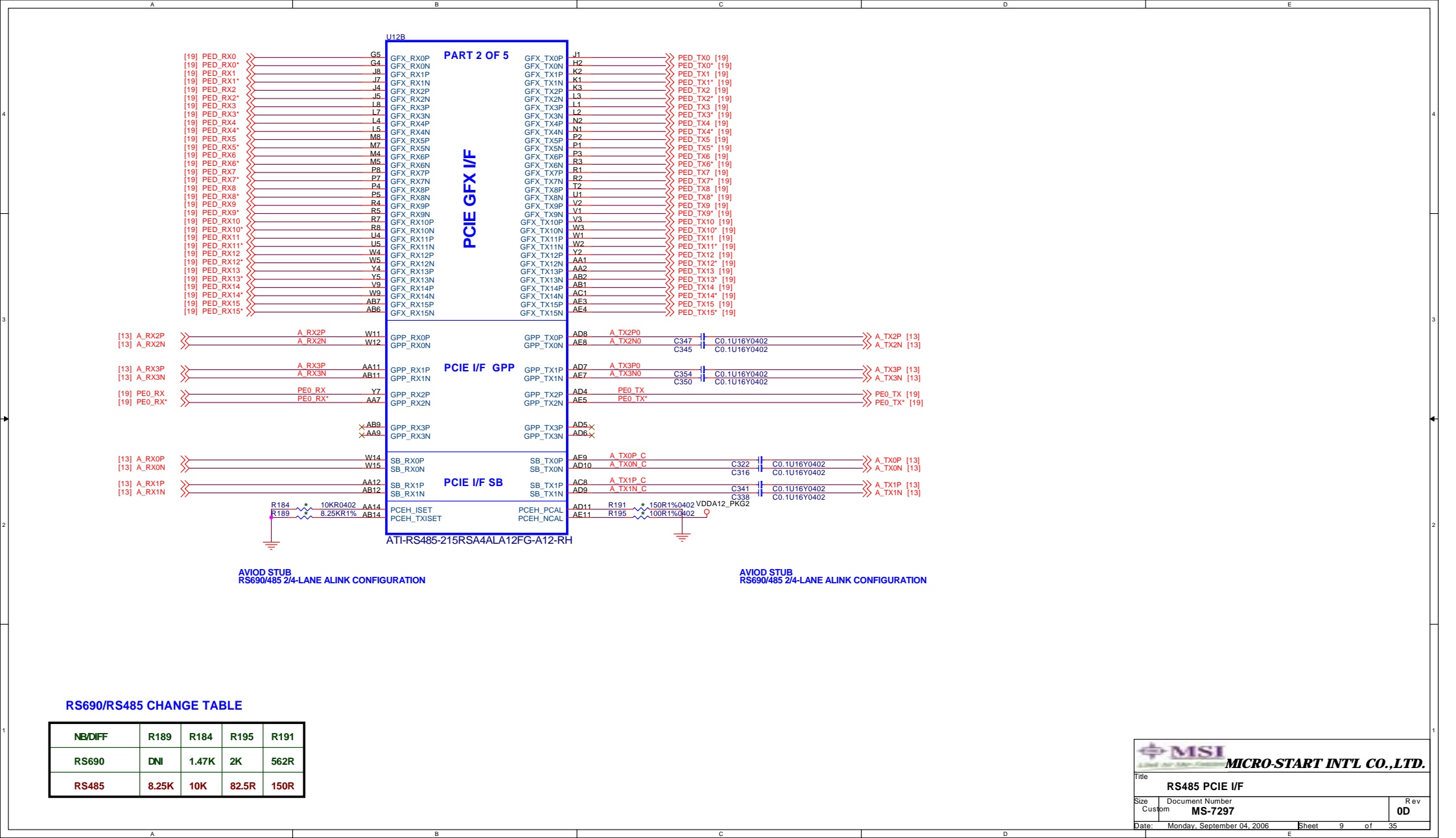
Layout: Spread out on VTT pour

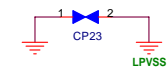


For EMI solution

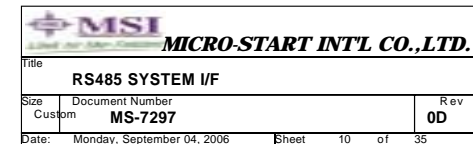








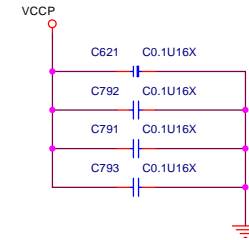
PART 3 OF 5



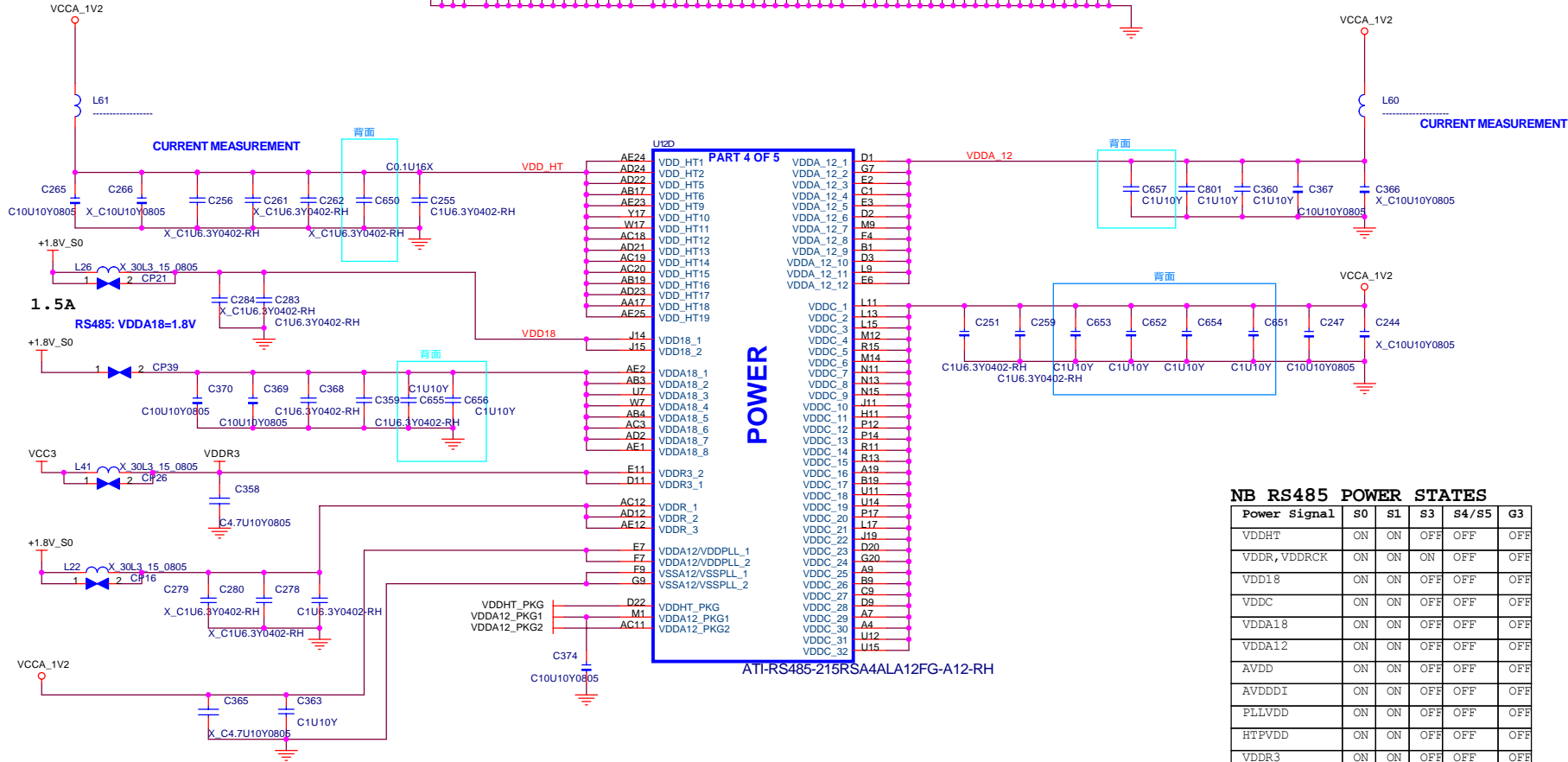
ATI-RS485-215RSA4ALA12FG-A12-RH

GROUND

PAR 5 OF 5



For EMI



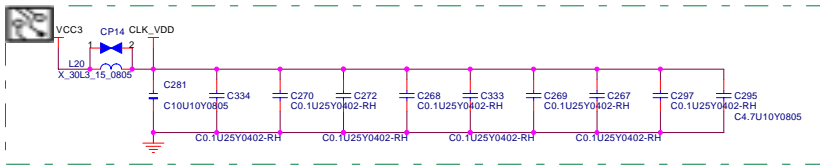
NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



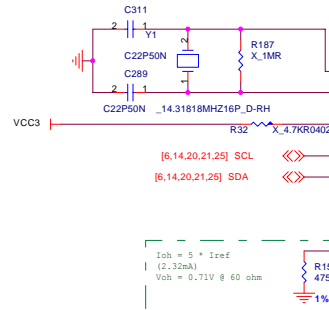
MICRO-START INT'L CO.,LTD.

Title			
RS485 POWER			
Size	Document Number		Rev
Custom	MS-7297		0D
Date:	Monday, September 04, 2006	Sheet	11 of 35



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U4 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U4 POWER PIN

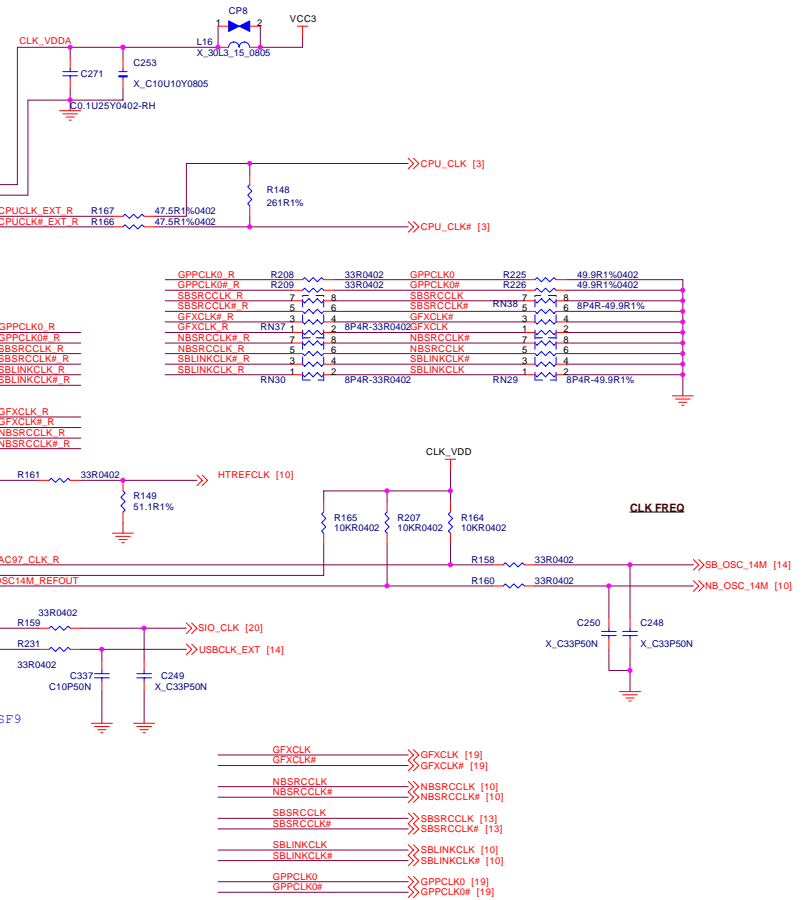
Parallel Resonance Crystal



I11-5146402-I02 & I11-8460702-SF9

OVERLAP COMMON PADS FOR DUAL-OP RESISTORS

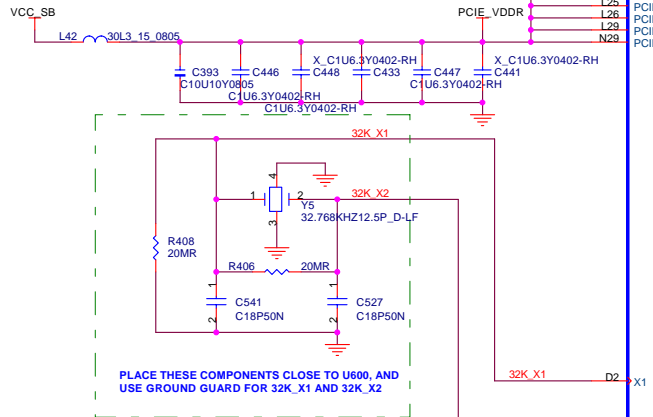
FS2	FS1	FS0	CPU	HTTCLK	SRC	ATIGCLK
0	0	0	Hi-Z	Hi-Z	100.0	100.0
0	0	1	REF	REF	100.0	100.0
0	1	0	230.0	76.7	100.0	100.0
0	1	1	240.0	80.0	100.0	100.0
1	0	0	100.0	66.6	100.0	100.0
1	0	1	133.3	66.6	100.0	100.0
1	1	0	166.6	66.6	100.0	100.0
1	1	1	200.0	66.6	100.0	100.0



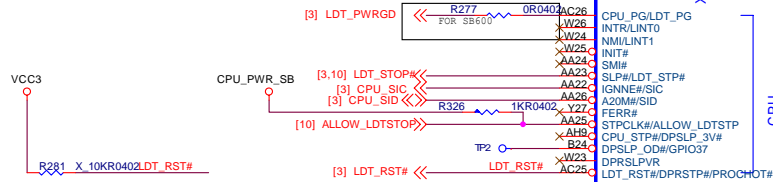
	SB CALIBRATION RESISTOR VALUE	
	SB600	SB460
R276	562 OHM 1%	150 OHM 1%
R293	2.05K 1%	150 OHM 1%
R322	0	4.12K 1%



FOR SB600 VCC_SB= 1.2V
FOR SB460 VCC_SB= 1.8V



PLACE THESE COMPONENTS CLOSE TO U600, AND
USE GROUND GUARD FOR 32K_X1 AND 32K_X2



ATI-SB600-218S6ECLA13FG-A13-RH



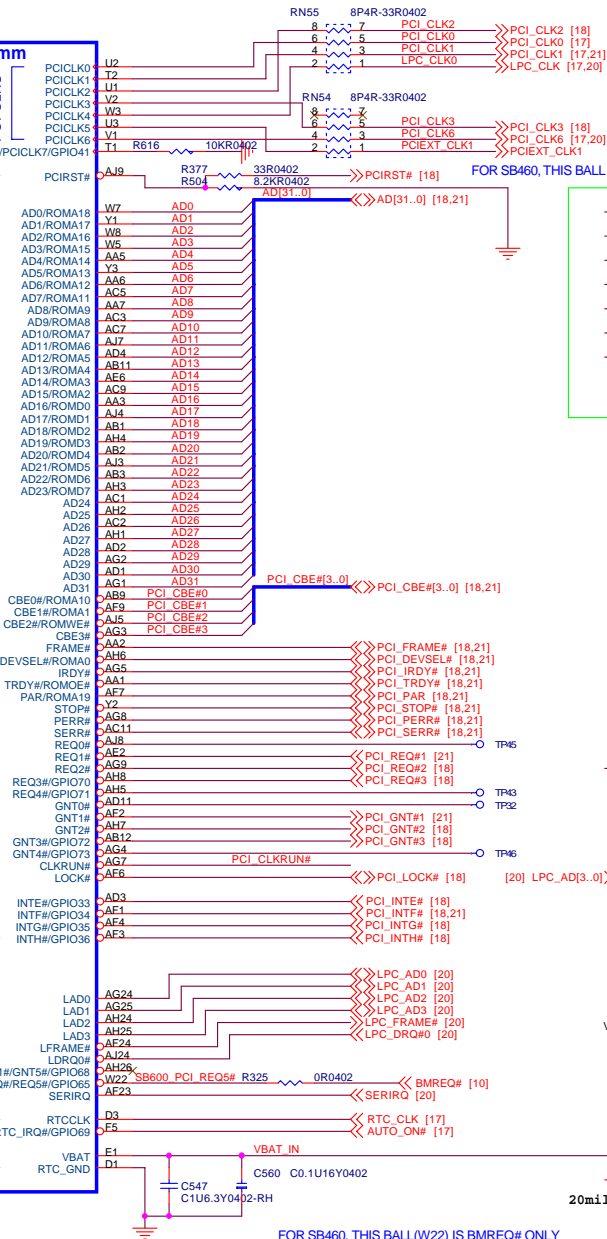
Part 1 of 4

PCI EXPRESS INTERFACE

PCI INTERFACE

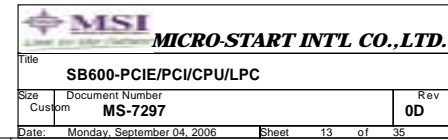
LPC

RTC



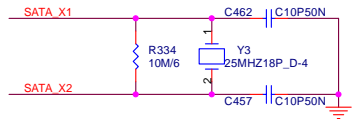
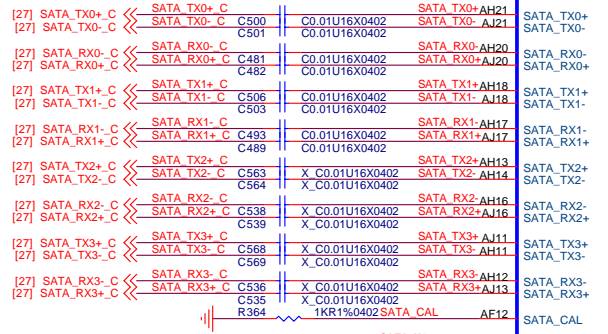
FOR SB460, THIS BALL(W22) IS BMREQ# ONLY

FOR SB600



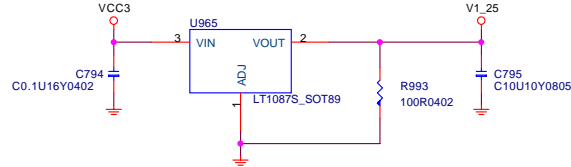


PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

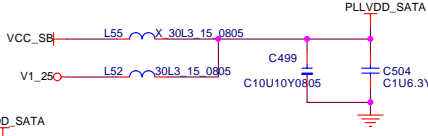


PLACE R364 CLOSE
TO U22 BALL

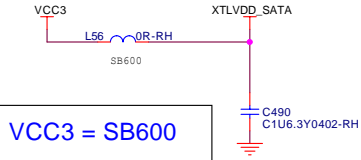
R364 IS 1K 1% FOR XTAL,
4.99K 1% FOR INTERNAL CLK



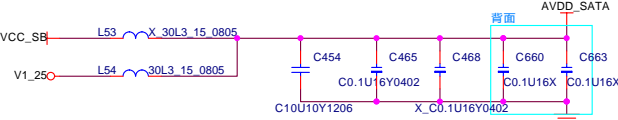
C490 CLOSE TO THE
BALL OF U22



C499 & C504 CLOSE
TO THE BALLS OF
U22



VCC3 = SB600



VCC_SB = 1.2V for SB600;

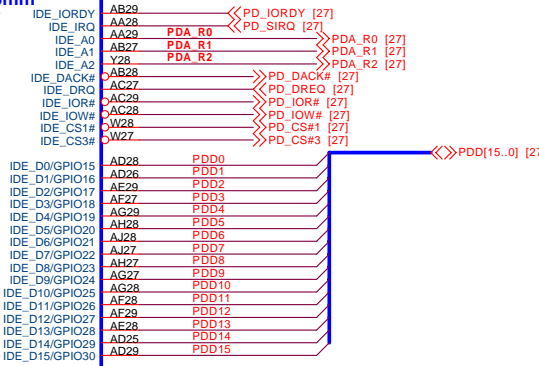
SB600 SB 23x23mm
Part 2 of 4

SERIAL ATA

SERIAL ATA POWER

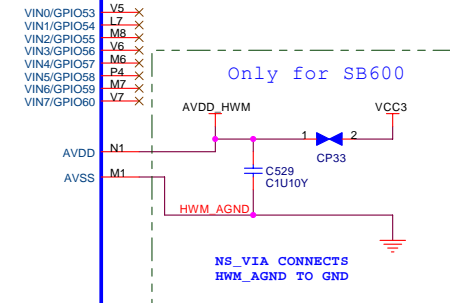
SPI ROM

HW MONITOR



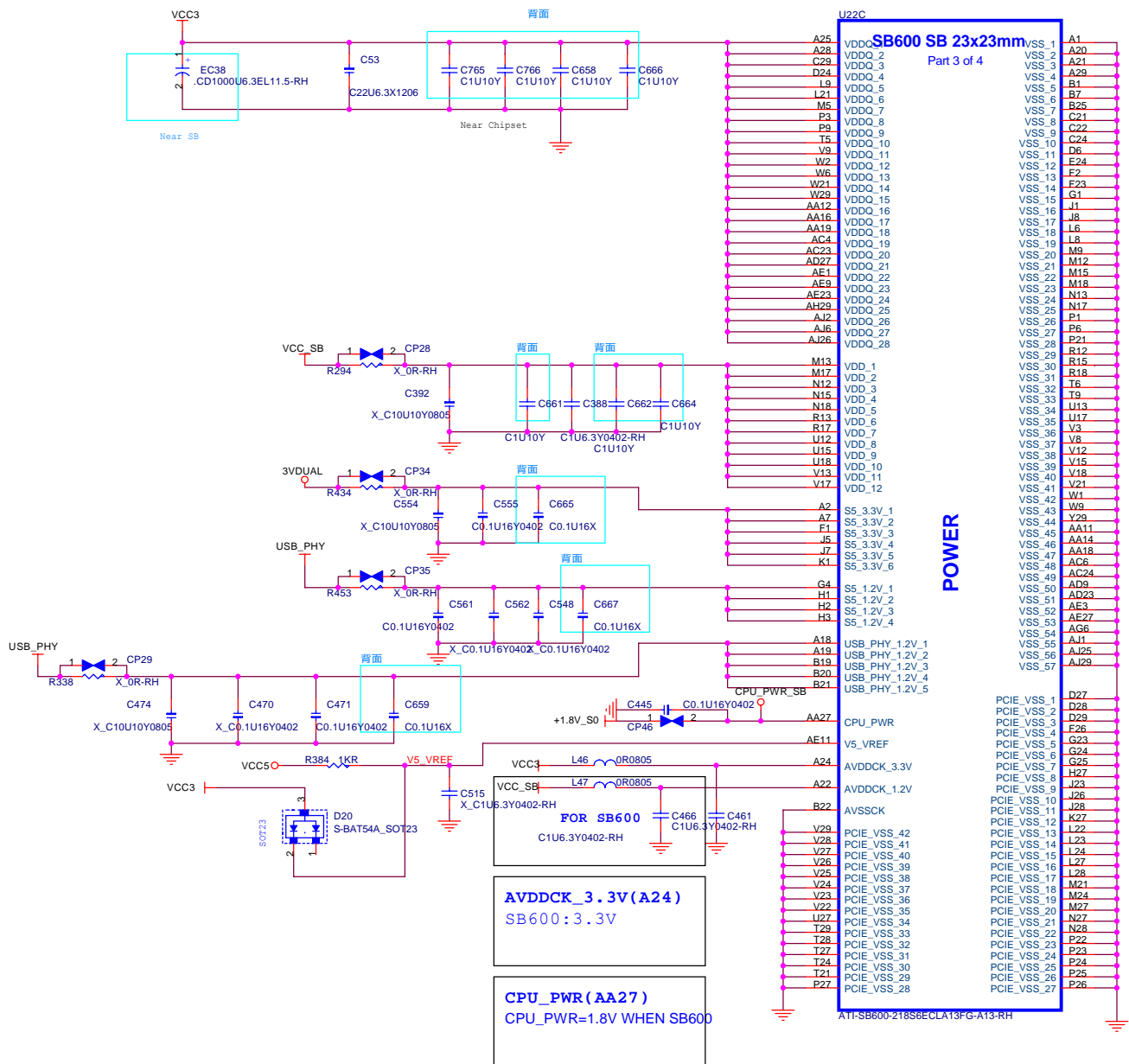
SPI ROM

HW MONITOR



Only for SB600

NS_VIA CONNECTS
HWM_AGND TO GND

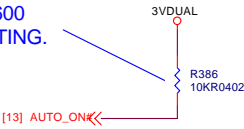
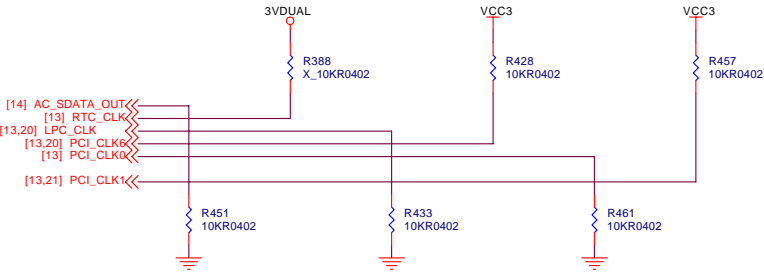




REQUIRED STRAPS

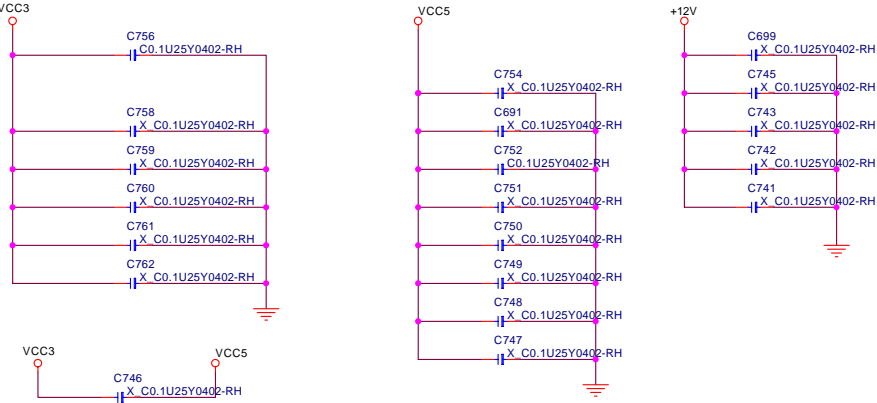
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED

NOTE: R386 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB600
TO KEEP THE INPUT FROM FLOATING.

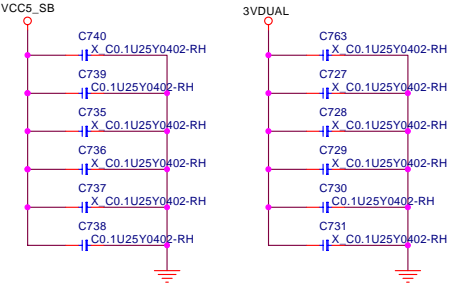


					SB600		SB460	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4				NOTE: FOR SB460, PCI0CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI0CLK[1:0]

For EMI



For EMI

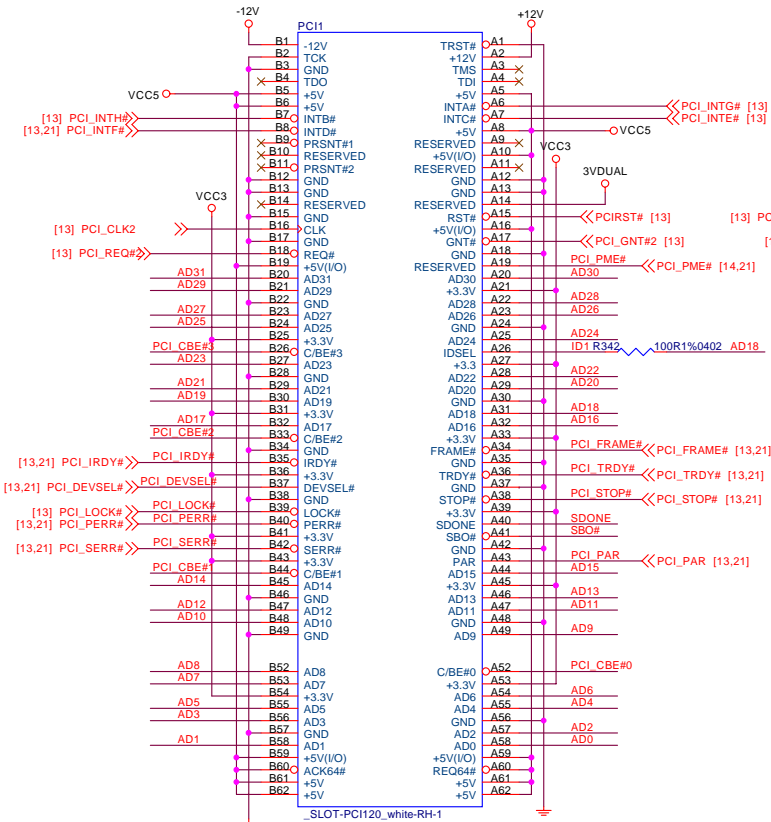


MICRO-START INTL CO.,LTD.

Title			SB600 STRAPS	
Size	Document Number	Rev		
Custom	MS-7297	0D		
Date:	Monday, September 04, 2006	Sheet	17	of 35

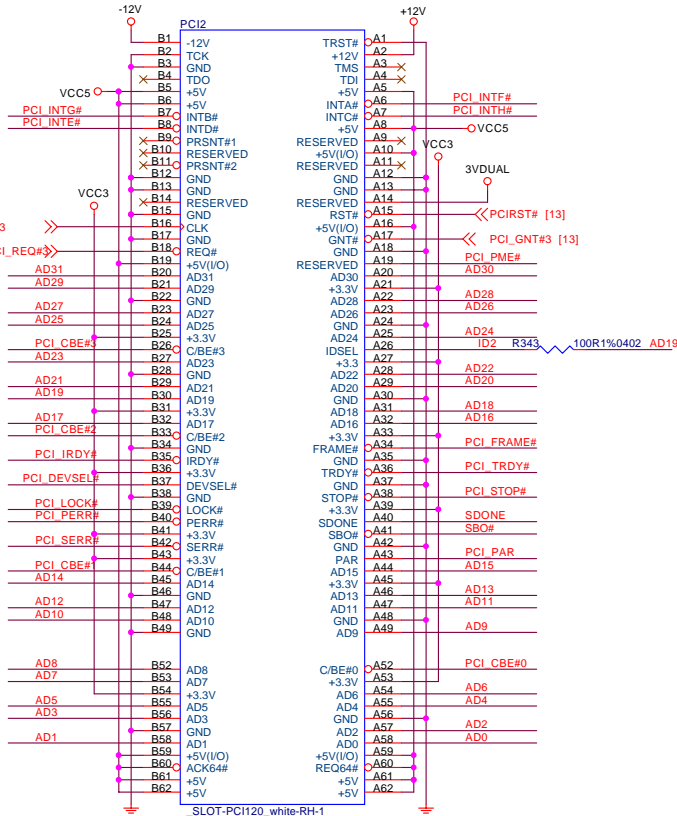
[13,21] AD[31..0] >> AD[31..0]
[13,21] PCI_CBE#[3..0] >> PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



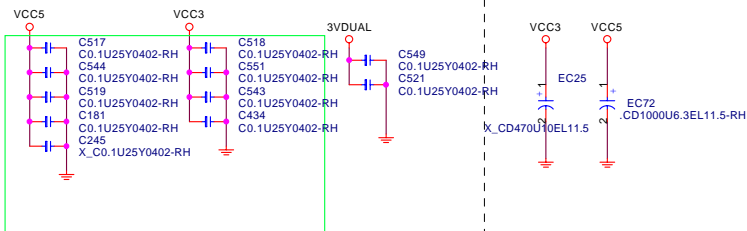
IDSEL = AD18
MASTER = PCI_REQ#2
PCI_GNT#2

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



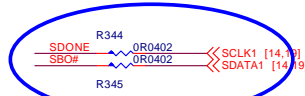
IDSEL = AD19
MASTER = PCI_REQ#3
PCI_GNT#3

PCI SLOT DECOUPLING CAPACITORS

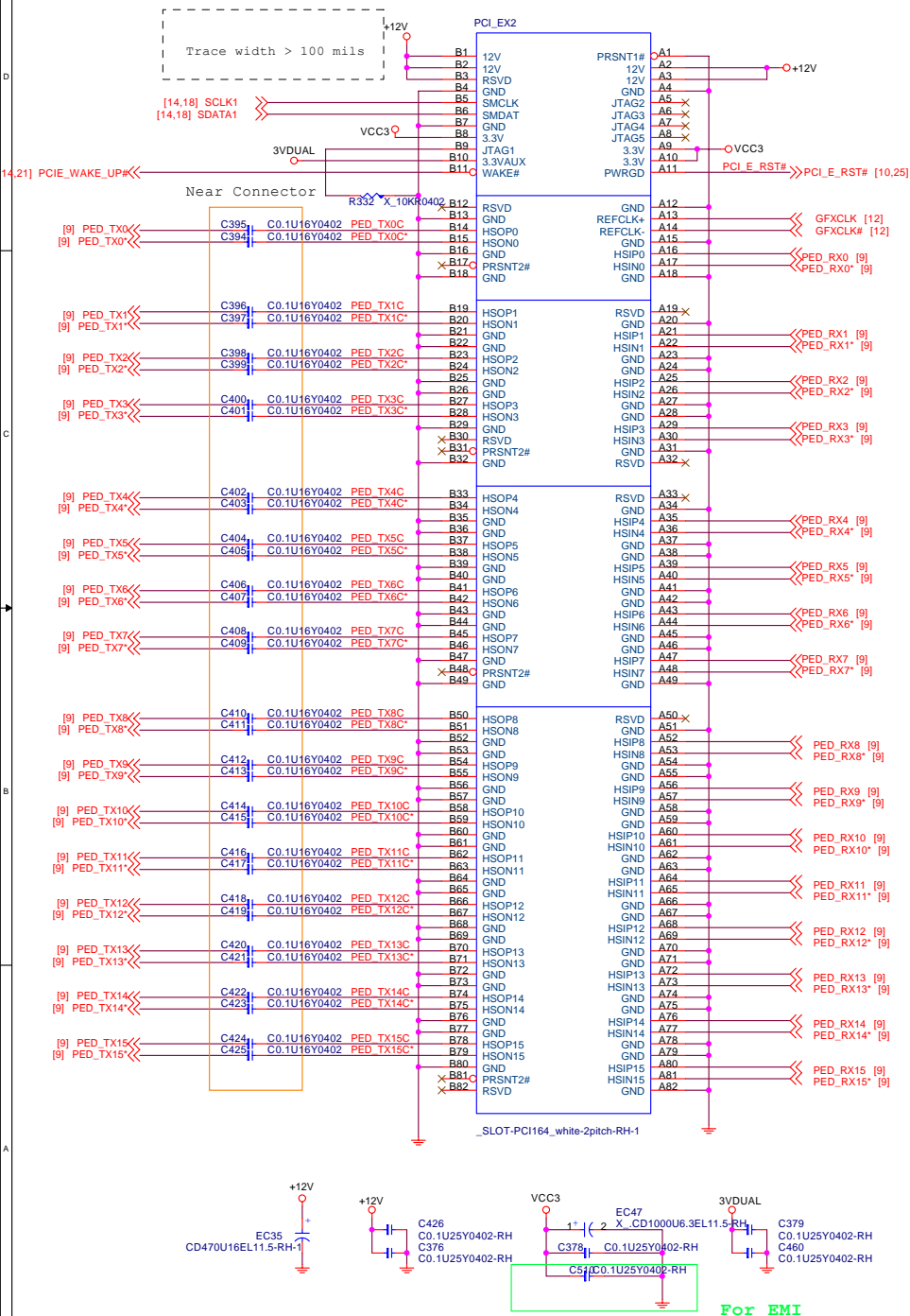


For EMI

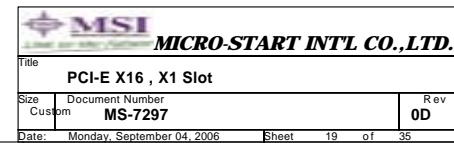
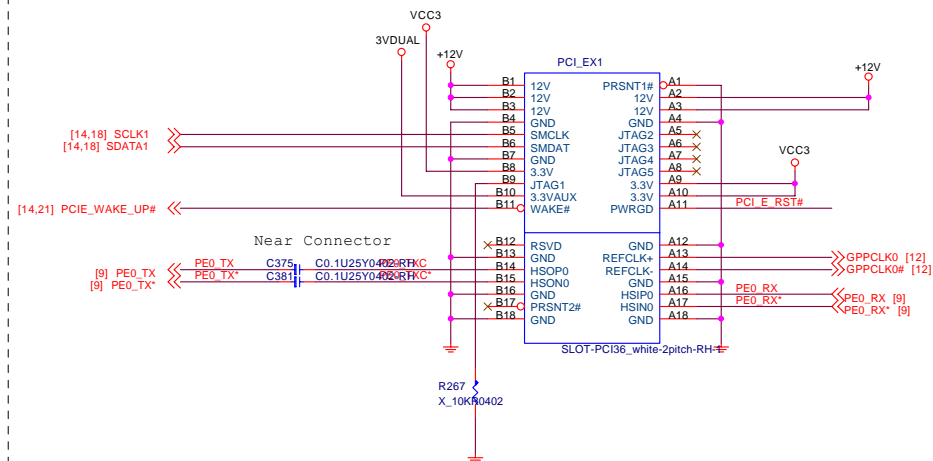
PCI PULL-UP / DOWN RESISTORS



PCI EXPRESS_16

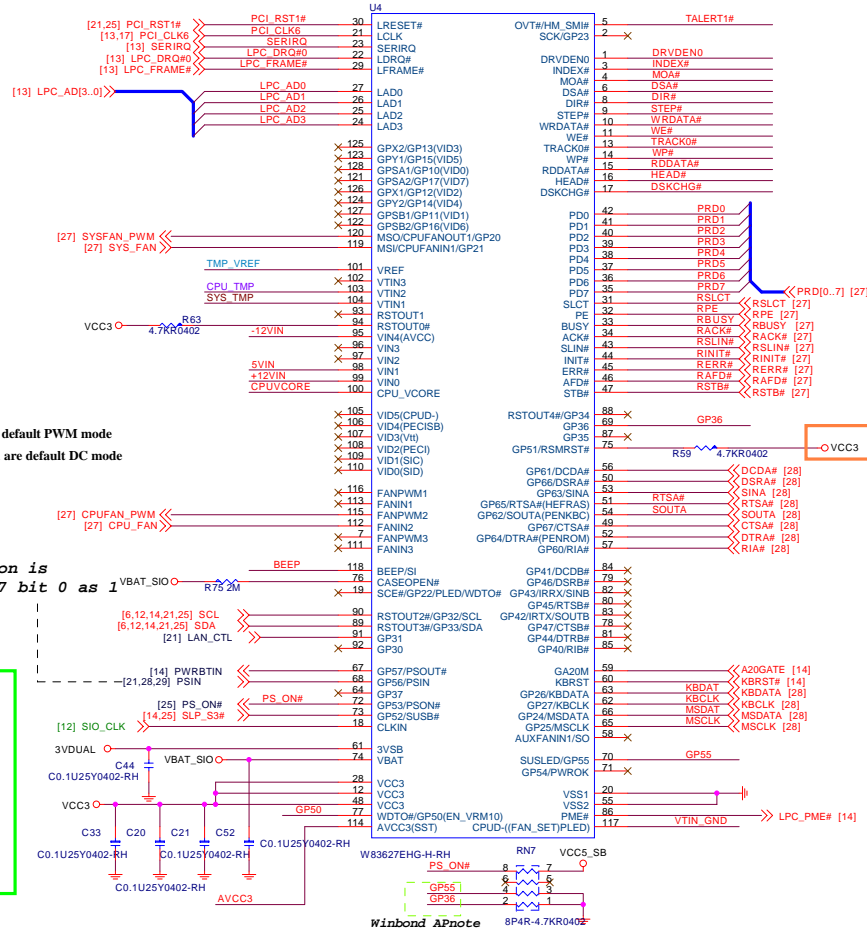


PCI-Express x1 SLO T 1

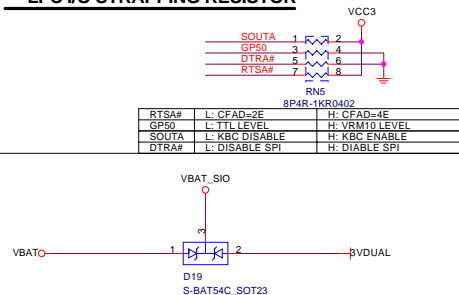


Super I/O

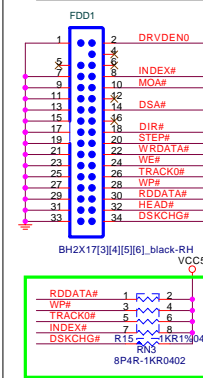
LPC SUPER I/O W83627EHG



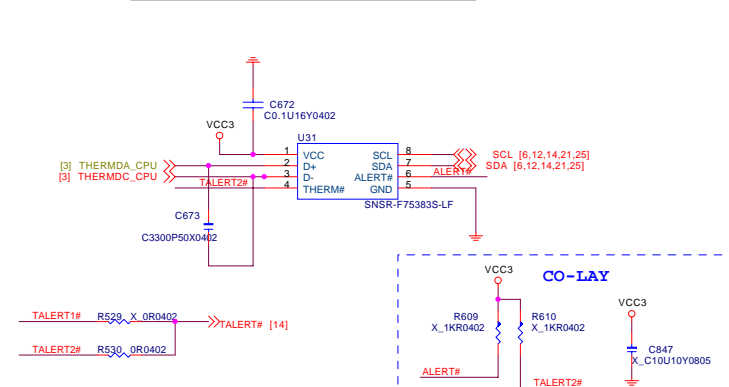
LPC I/O STRAPPING RESISTOR



FLOPPY CONNECTOR

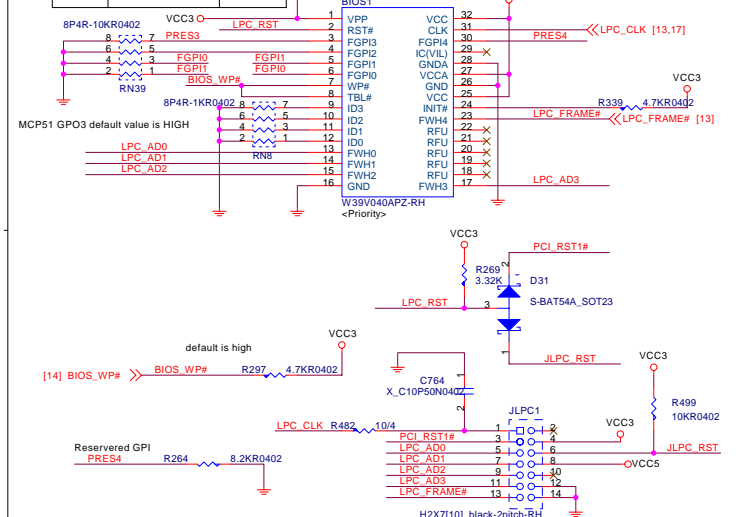


CPU TEMPERATURE SENSOR

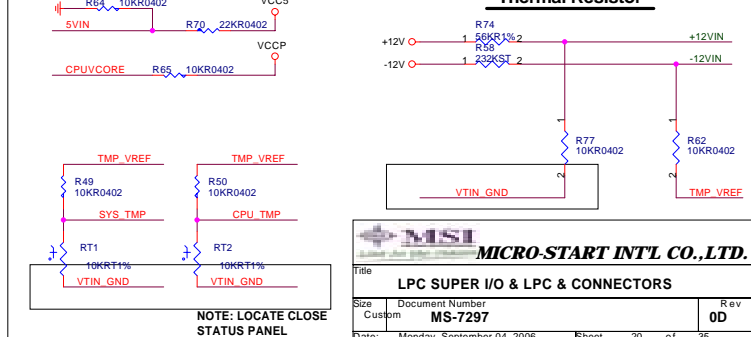


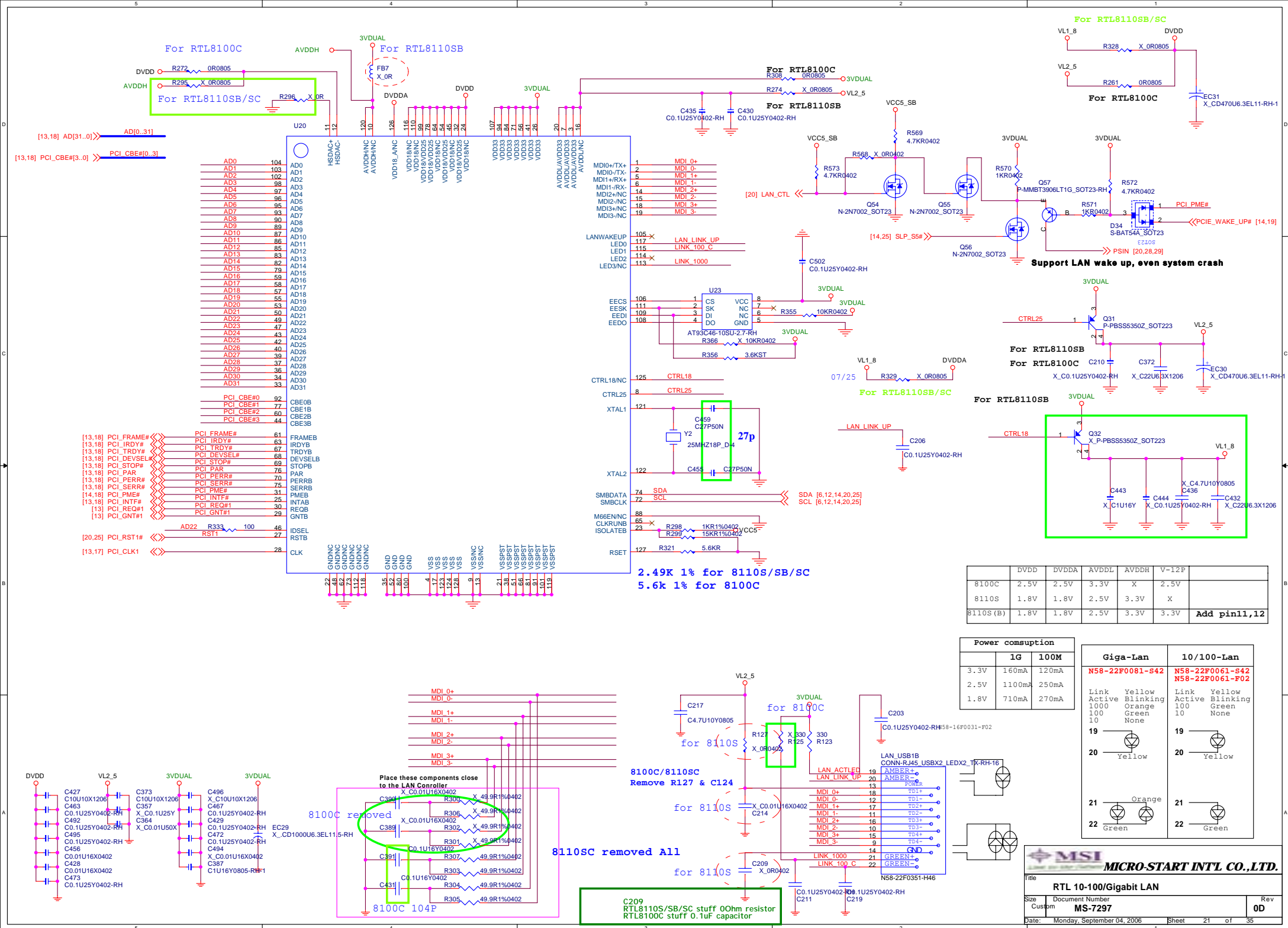
BIOS PROTECT BLOCK

BIOS Update Config.		
HIGH	Un_protected	Default
LOW	Protected	

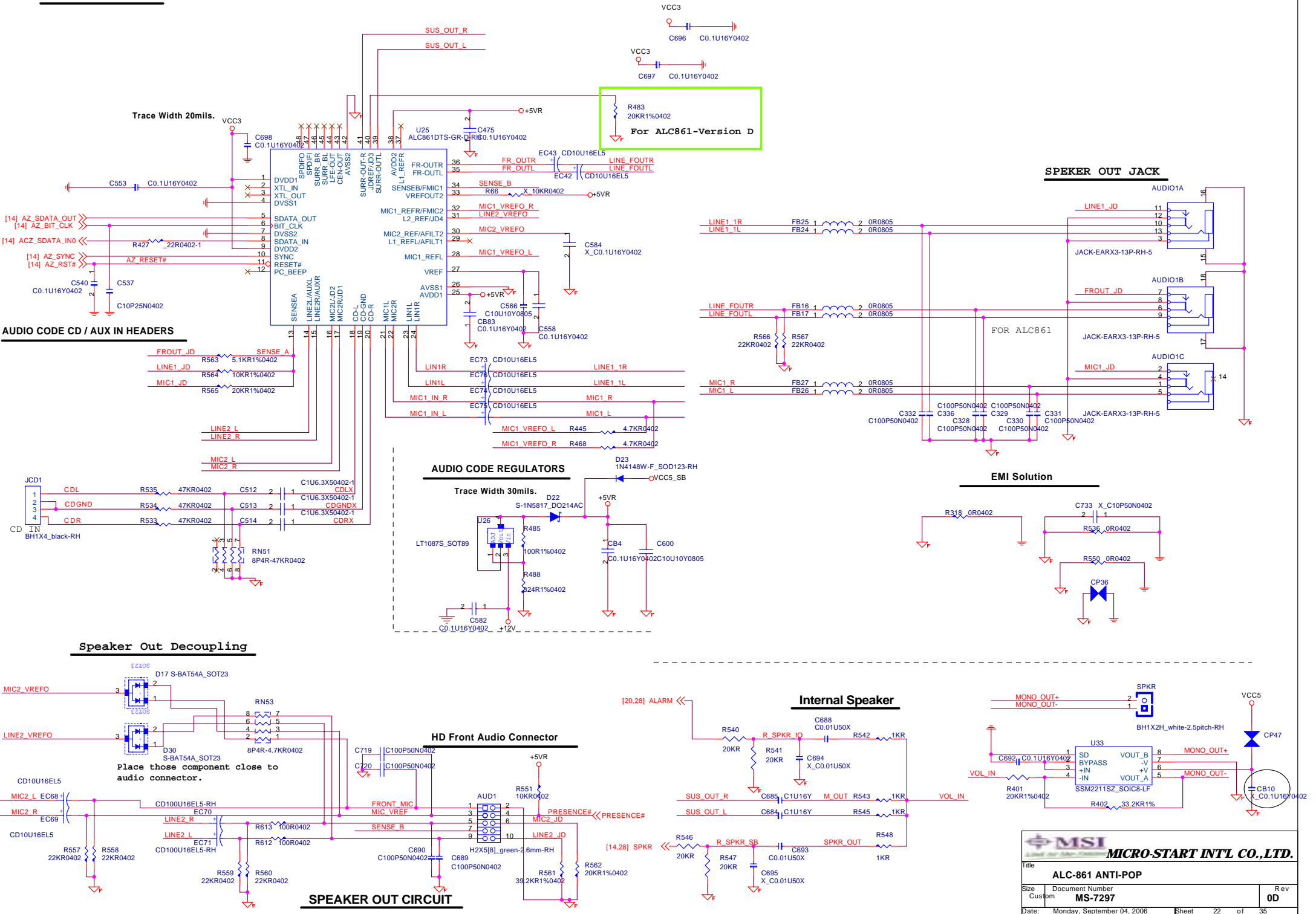


Thermal Resistor





ALC861 CODEC



[illegible]

The schematic diagram illustrates the USB front panel connector circuit. It features a +5VUSB_FRONT1 input connected to a 120 mils trace. This trace passes through a 5.1K/6 resistor (R486) and a 0.1uF capacitor (C615) to the FRONT USB CONNECTOR. A 10KR0402 resistor (R487) is connected to the connector. A note indicates a 14-pin connector (U14) is used for USB_OC#5. A component EC41 (CD1000U6.3EL11.5-RH) is also shown.

The schematic diagram illustrates the electrical connections for the USB connector area. It includes the following components and connections:

- ESD Protection:** A network of diodes and a capacitor (D13, X_ESD-IP4220) connected to the SVCC1 supply and the USB27 component.
- USB27 (CMC-L12-181D017-LF):** A component with 8 pins. The connections are:
 - Pin 1: USBP2 (red)
 - Pin 2: SBD2+ (blue)
 - Pin 3: USBN2 (red)
 - Pin 4: SBD2- (blue)
 - Pin 5: USBP3 (red)
 - Pin 6: SBD3+ (blue)
 - Pin 7: USBN3 (red)
 - Pin 8: SBD3- (blue)
- LAN_USB1A:** A component with 10 pins. The connections are:
 - Pin 5: SBD3- (blue)
 - Pin 6: SBD3+ (blue)
 - Pin 7: SBD3- (blue)
 - Pin 8: SBD3+ (blue)
 - Pin 1: SBD2- (blue)
 - Pin 2: SBD2+ (blue)
 - Pin 3: SBD2- (blue)
 - Pin 4: SBD2+ (blue)
 - Pin 23: SVCC1 (red)
 - Pin 24: GND (red)
 - Pin 25: GND (red)
 - Pin 26: GND (red)
 - Pin 27: GND (red)
 - Pin 28: GND (red)
 - Pin 29: GND (red)
 - Pin 30: GND (red)

ESD Protection

The diagram illustrates two ESD protection circuit options for USB port 2,3. Both options are connected to SVCC1 and ground.

Option 1 (Left): Uses a diode array (D15, X_ESD-IP4220). The circuit is connected to SVCC1 and ground. The connections are as follows:

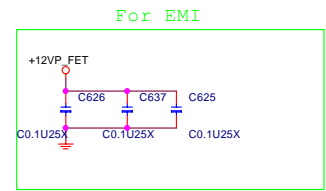
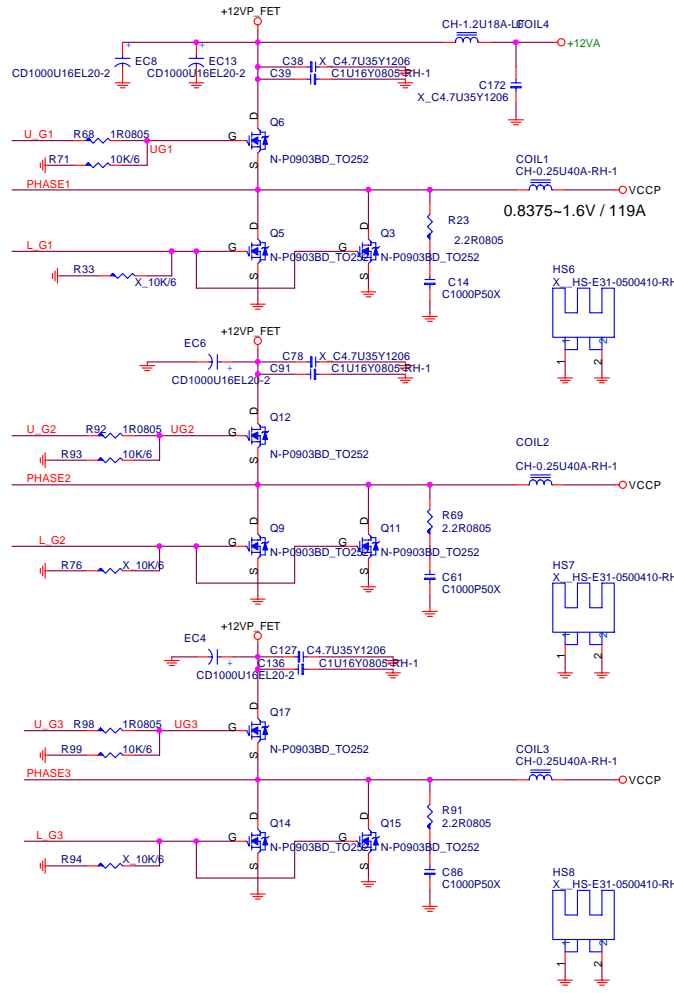
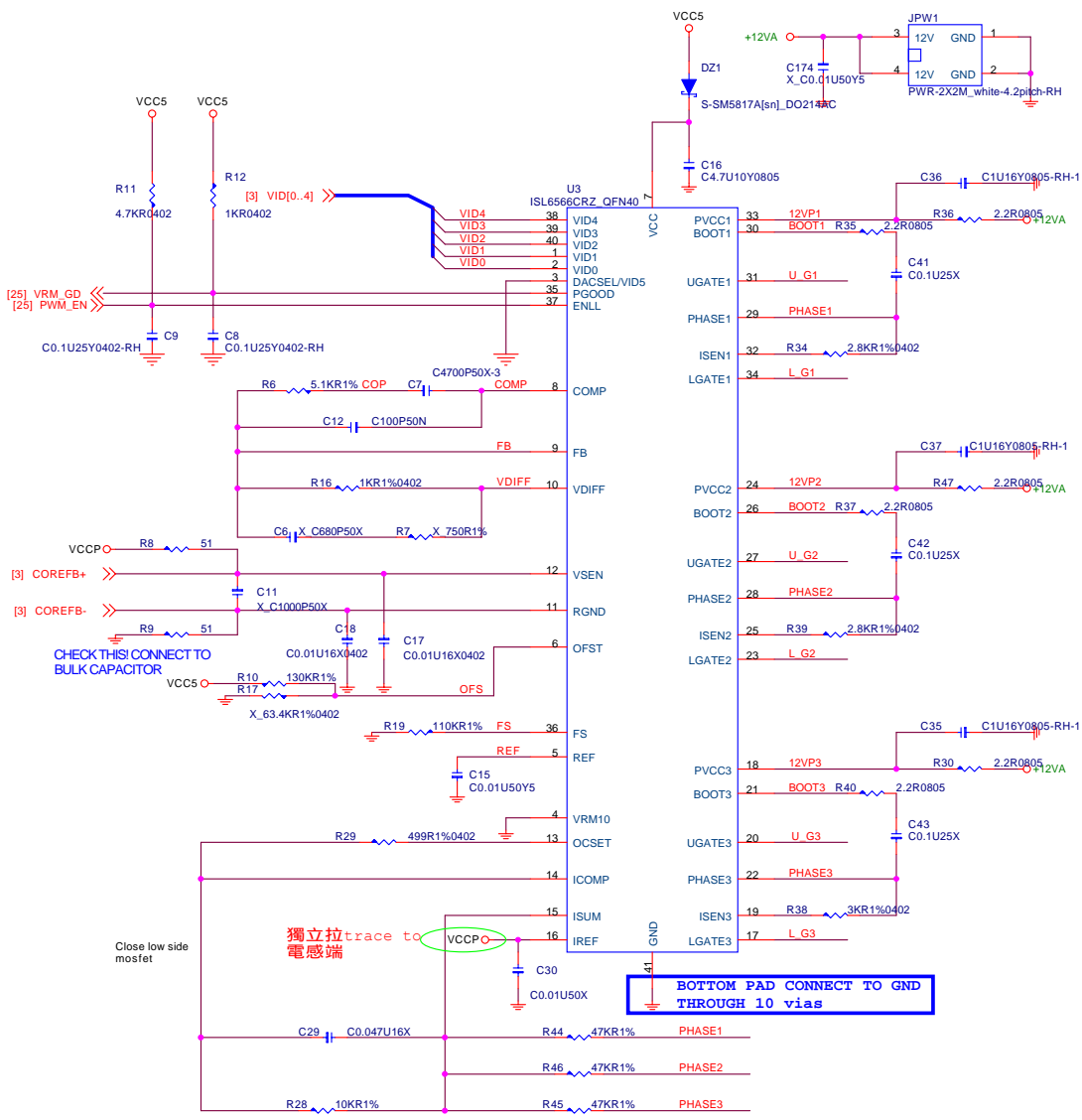
- SBD1+ (pin 6) connects to pin 1 of the diode array.
- SBD1- (pin 1) connects to pin 2 of the diode array.
- SBD0+ (pin 4) connects to pin 3 of the diode array.
- SBD0- (pin 3) connects to pin 4 of the diode array.

Option 2 (Right): Uses two N-channel MOSFETs (UP and DOWN, N53-08M0261-H46). The circuit is connected to SVCC1 and ground. The connections are as follows:

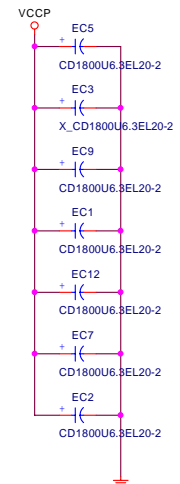
- SBD1+ (pin 6) connects to pin 11 of the UP MOSFET.
- SBD1- (pin 1) connects to pin 5 of the UP MOSFET.
- SBD0+ (pin 4) connects to pin 7 of the DOWN MOSFET.
- SBD0- (pin 3) connects to pin 8 of the DOWN MOSFET.

Voltage Regular
Module

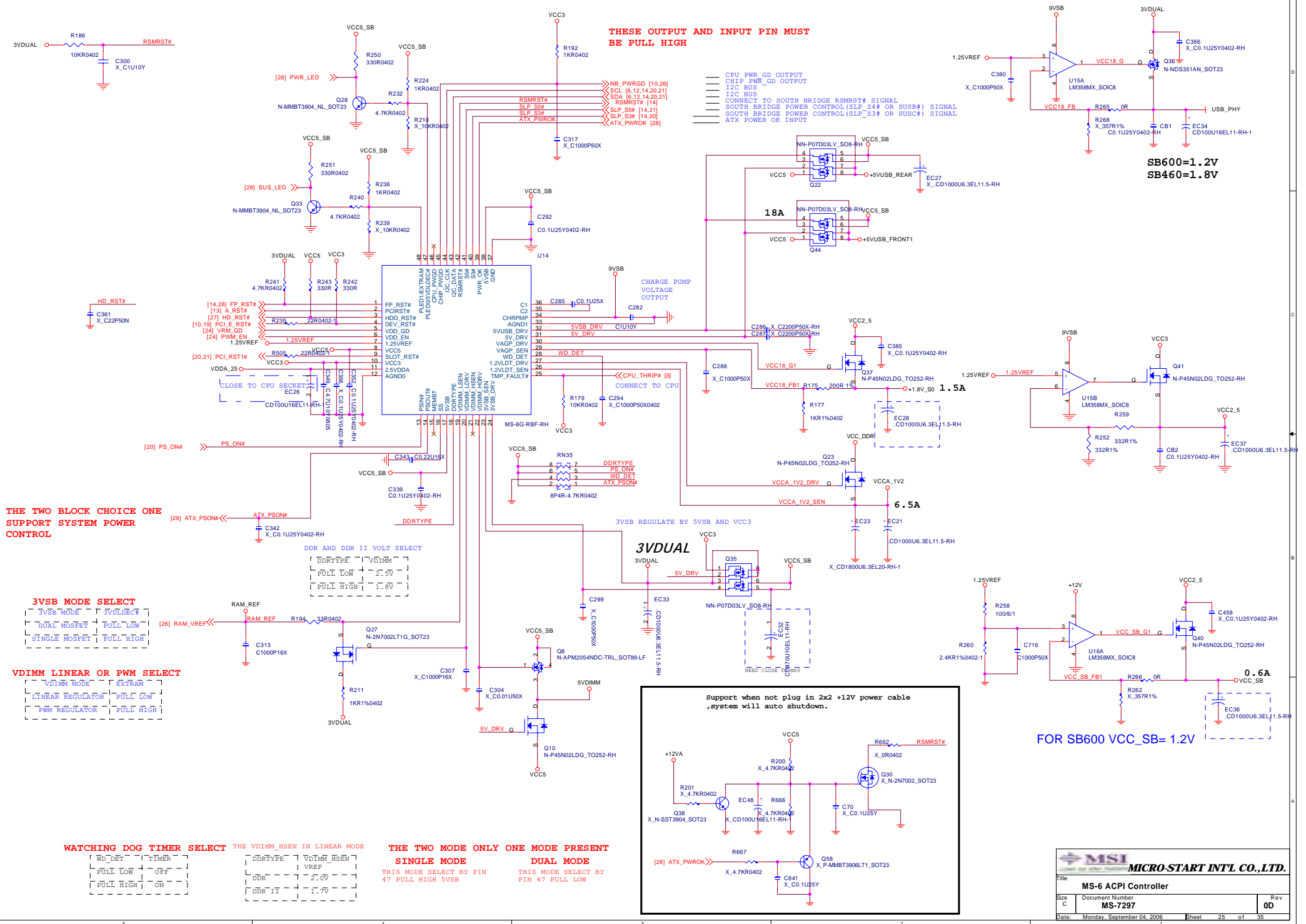
IPF06N03LA Rds(on)=8.7mΩ (@4.5V, 30A), Vgs(on)=1.2~2V, Id=50A, Ciss=3110pf, Qg=10nC, Vds=25V, Vgs=±20V
C100U2SP ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C
.CD3300U6.3EL25 ESR<12mΩ, Ripplecur.<2800mA, 105C, longlife3000hrs, KZGSeries
560u_2.5V ESR=6mΩ, Ripplecur.=4400mA, Lc.<500uA, 105C/2000hrs
1800UF/6.3V ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.6uH/40A 0.6u/20%, Isat=40A, Rdc=1.2m ohm, PEW wire
CH-1.2U18A 1.2u/20%, Dip-2/vertical17.5mm, 1.2ψ/5.5turns, 18A



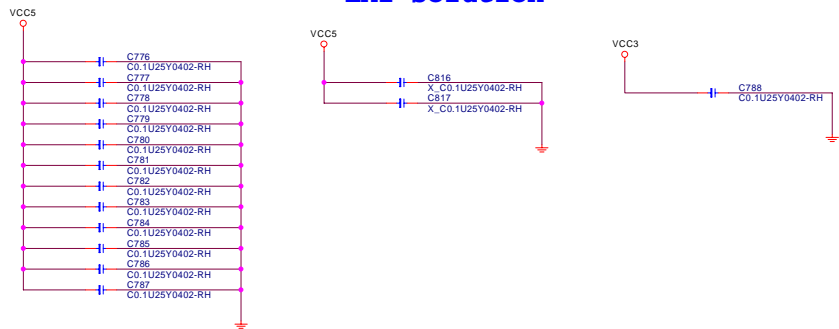
EL Capacitors



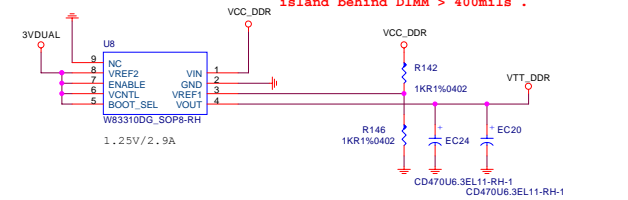
PWM MODE



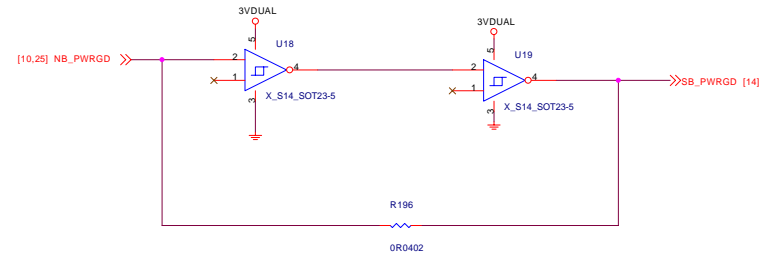
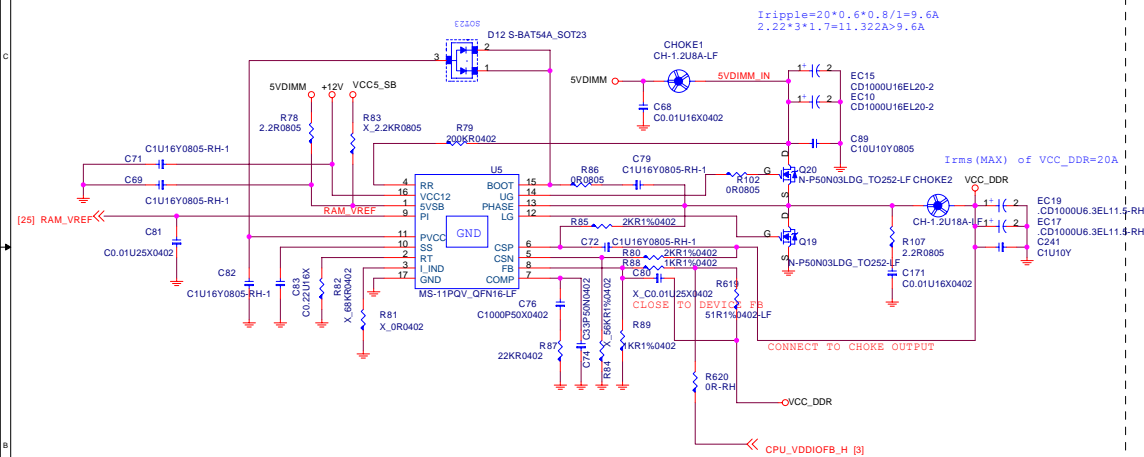
EMI solution



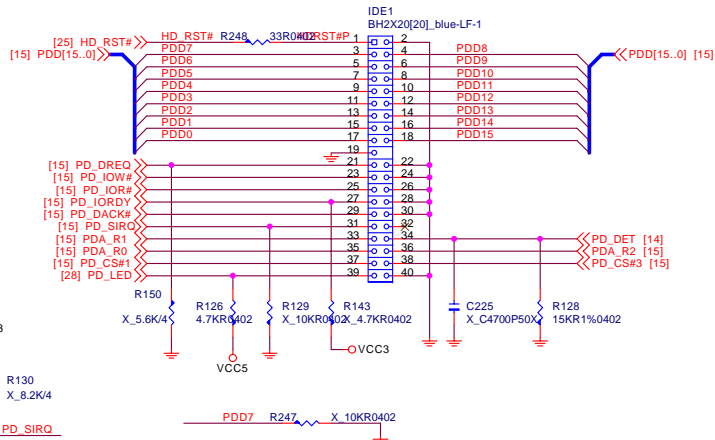
DDR VTT Power



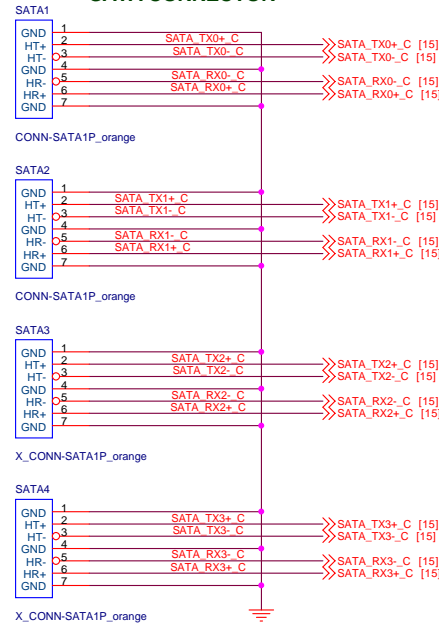
DDR II 1.8V POWER



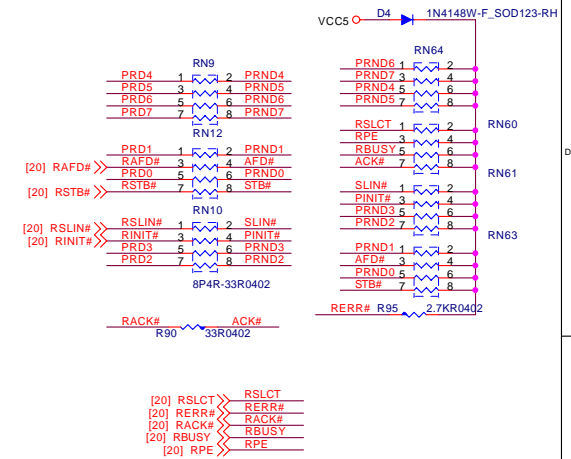
IDE 1



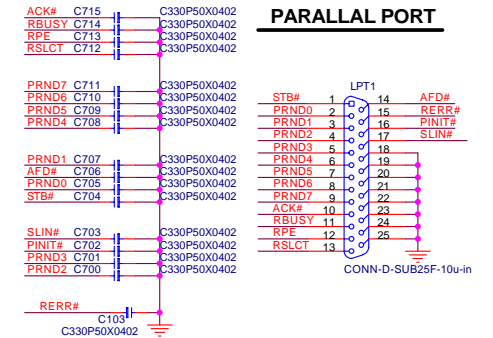
SATA CONNECTOR



[20] PRD[0..7] >> PRD[0..7]

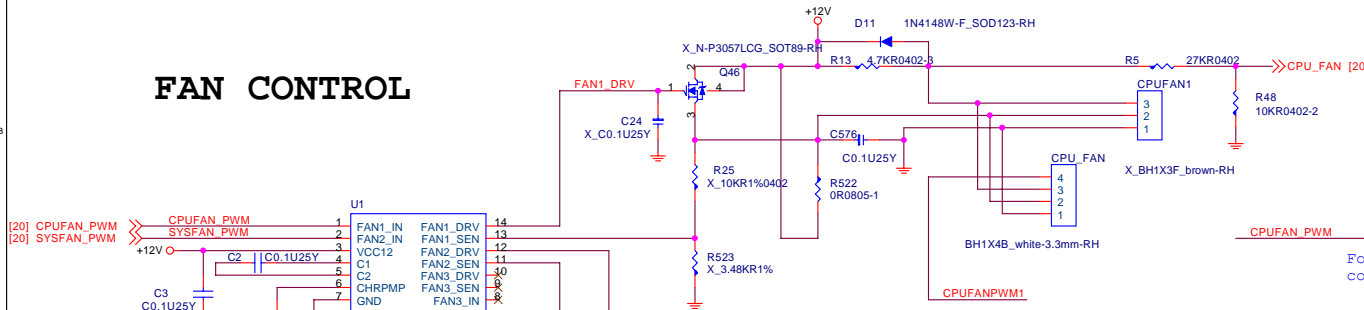


PARALLAL PORT

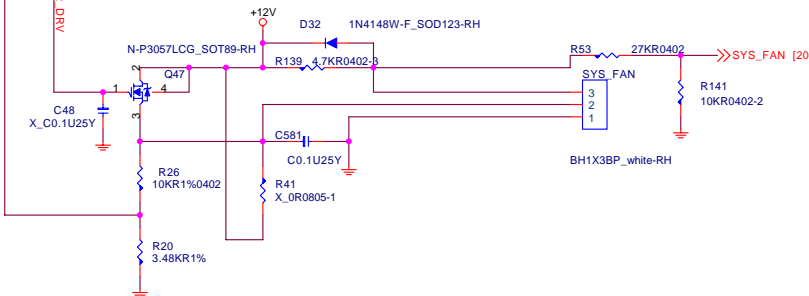


FAN CONTROL

CPU FAN



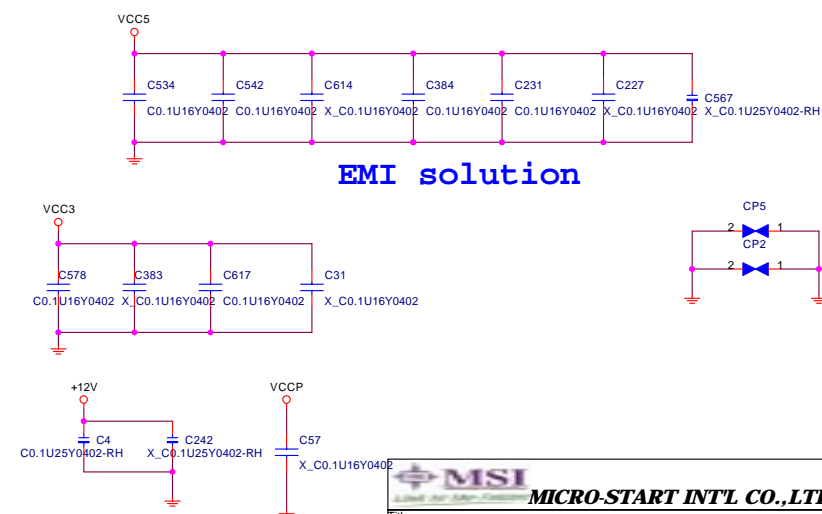
SYSTEM FAN



R1 value might need to be tuned for EOS and compatibility

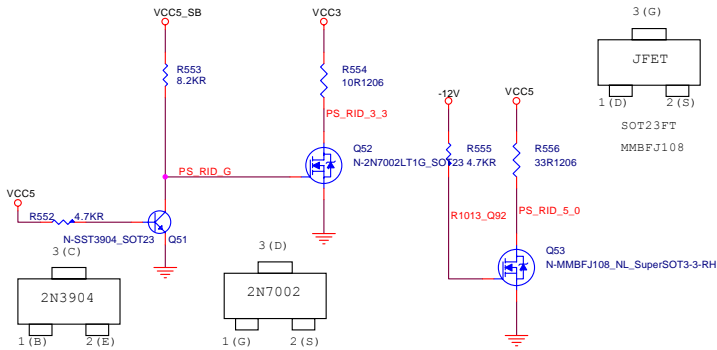
For open-drain (Ver.H) control signal

Intel Front Panel

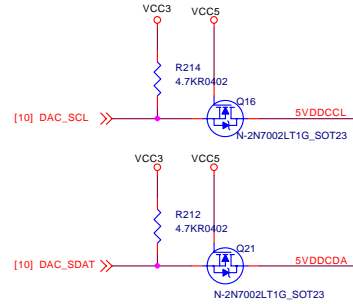
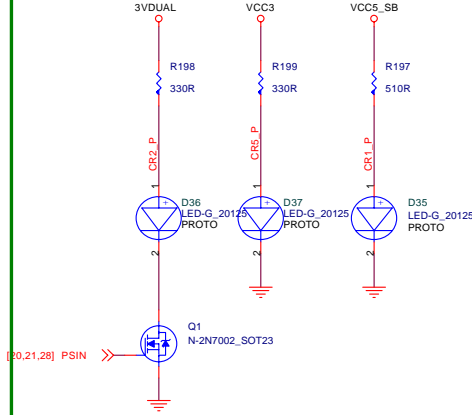


Near ATX POWER Connector

BLEED-OFF CIRCUIT

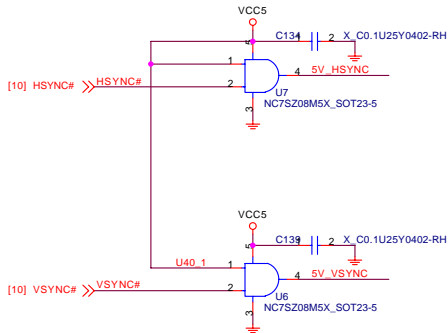
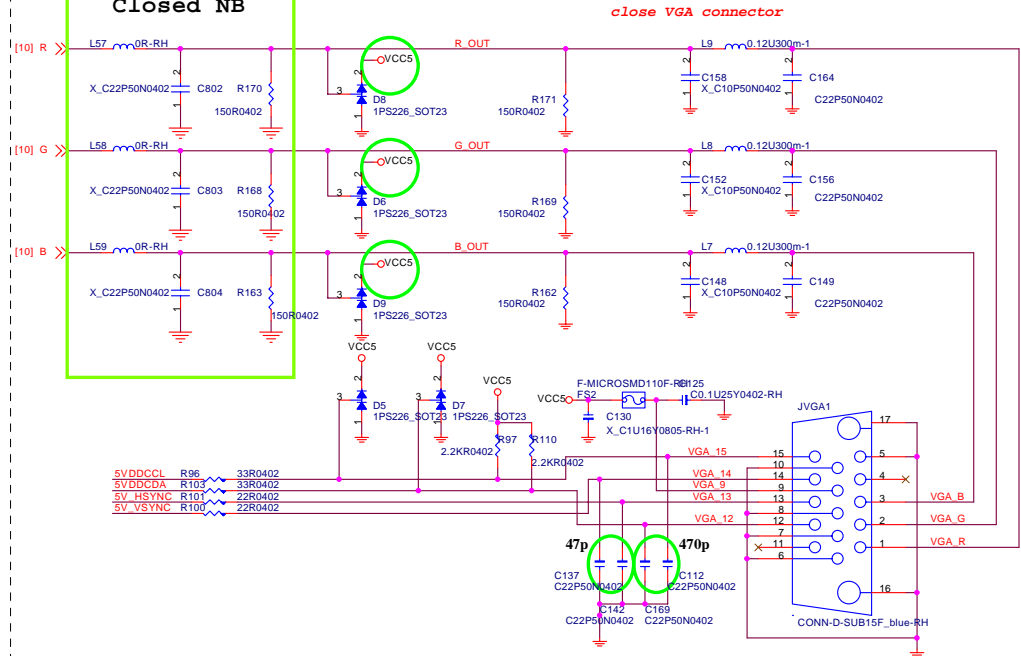


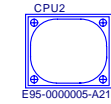
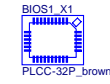
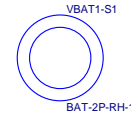
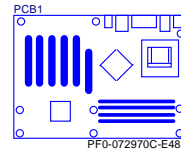
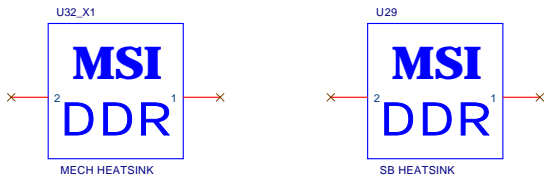
DESIGN NOTE: THIS CIRCUIT IS USED TO BLEED OFF 5.0V & 3.3V



VGA CONNECTOR

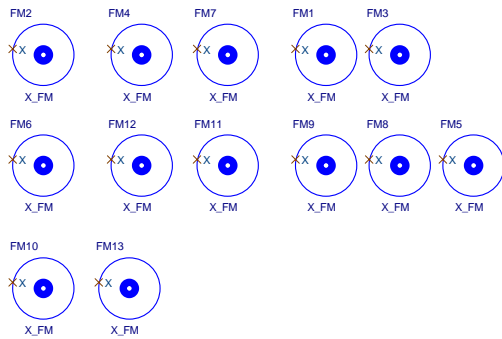
Closed NE



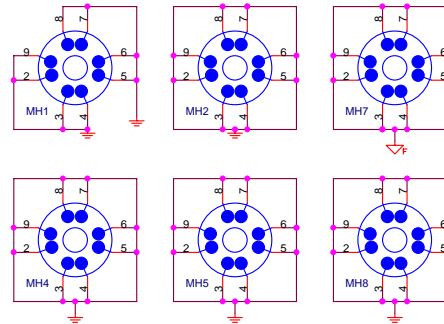


PF0-072970C-E48, 競華, 107, 寶安恩斯通廠 (MSIS)
PF0-072970C-E48, 競華, 23, 寶安恩斯通廠 (MSIS)
PF0-072970C-G37, 精成, 107, 寶安恩斯通廠 (MSIS)
PF0-072970C-G37, 精成, 23, 寶安恩斯通廠 (MSIS)

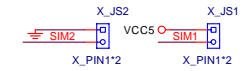
Optics Orientation Holes



Mounting Holes



Simulation



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7297	RS485+SB600+RTL8110SB+ALC861+2PCI+u-ATX +2PS2+8USB+1COM+VGA+1Audio+LPT+RJ45	cfg-7297-0A	601-7297-01S